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Application Number	10/665,289-Conf. #5629
Filing Date	September 22, 2003
First Named Inventor	Robert J. Devins, Esq.
Art Unit	2671
Examiner Name	J. Hsu
Attorney Docket Number	21806-00056-US1

ENCLOSURES (*Check all that apply*)

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- [ ] Amendment/Reply
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  - [ ] Affidavits/declaration(s)
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- [x] Other Enclosure(s) (please identify below):

Pre-Appeal Brief Request for Review

Arguments for Pre-Appeal Brief Review

Remarks: Notice of Appeal and Request for Pre-Appeal Brief Review enclosed

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	CONNOLLY BOVE LODGE & HUTZ LLP		
Signature	Larry J. Hume		
Printed name	Larry J. Hume		
Date	February 14, 2006	Reg. No.	44,163

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FAX TRANSMISSION

DATE: February 14, 2006

PTO IDENTIFIER: **Application Number** 10/665,289-Conf. #5629
Patent Number
Inventor: Robert J. Devins, Esq. et al.

MESSAGE TO: US Patent and Trademark Office (MS AF)
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FROM: CONNOLLY BOVE LODGE & HUTZ LLP
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Attorney Dkt. #: 21806-00056-US1

PAGES (Including Cover Sheet): 10

CONTENTS:
Notice of Appeal (1 page)
Pre-Appeal Brief Request for Review (1 page)
Arguments for Pre-Appeal Brief Review (5 pages)
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PAGE 1/10 * RCVD AT 2/14/2006 5:17:21 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/24 * DNIS:2738300 * CSID:202 293 6229 * DURATION (mm-ss):02-52

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Application No. (if known): 10/665,289 Attorney Docket No.: 21806-00056-US1

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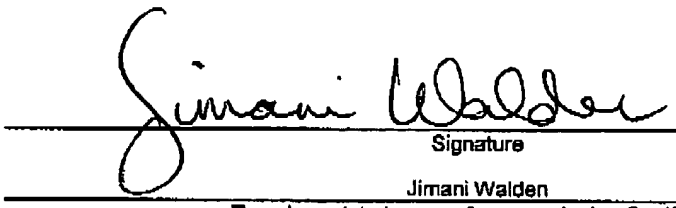

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PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) 21806-00056-US1	
	Application Number 10/665,289-Conf. #5629	Filed September 22, 2003
	First Named Inventor Robert J. Devins, Esq. et al.	
	Art Unit 2671	Examiner J. Hsu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant /inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [ ] attorney or agent of record. Registration number _____
- [x] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. 44,163

Larry J. Hume
Signature

Larry J. Hume
Typed or printed name

(202) 331-7111
Telephone number

February 14, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of 1 forms are submitted.

Docket No.: 21806-00056-US1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Robert J. Devins et al.
Application No.: 10/665,289

Confirmation No.: 5629

Filed: September 22, 2003

Art Unit: 2671

For: METHOD AND SYSTEM FOR GRAPHICS RENDERING USING HARDWARE-EVENT-TRIGGERED EXECUTION OF CAPTURED GRAPHICS HARDWARE INSTRUCTIONS

Examiner: J. Hsu

ARGUMENTS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 14, 2006

Dear Sir:

Claims 29-37 remain pending in this application and are the subject of this Pre-Appeal Brief Request for Review, filed concurrently with the Notice of Appeal.

Claims 29 and 34 are independent.

I. Peaslee in View of Dye do not Teach or Suggest all Claim Limitations

Reversal of the rejection of claims 29-37 under 35 U.S.C. §103(a) as being unpatentable over Peaslee (US 5,276,798) in view of Dye (US 5,706,478) is requested. The applied art does not teach or suggest all the claimed limitations, in particular, the limitations of independent claims 29 and 34.

A. Claim 29

1. Without hardware interrupt processing by the host system

The applied art, taken alone or in combination, does not teach or suggest a method for offloading hardware interrupt processing from a host system to a subsystem which includes, among other features, "...utilizing a subsystem processor to execute the executable program with subsystem hardware without hardware interrupt processing by the host system...", as recited in independent claim 29.

Peaslee teaches away from this limitation by disclosing that the CPU is coupled to the subsystem (DLP 28) via interrupt lines. *See* Peaslee at col. 6, lines 21-27 and FIG. 5. The display list command interpreter 93 provides the functions of a concurrent processing circuit, an interrupt input circuit, and a restore control circuit. The interrupt handler address generator 97 provides the functions of an interrupt input circuit, a nested interrupt input circuit, a restore execution circuit, and a multilevel nested interrupt circuit. *See* Peaslee at col. 6, lines 32-38 and FIG. 5.

Thus, Peaslee teaches that the interrupt is at least ***generated*** by the CPU, if not "handled".

2. **Subsystem status indicator**

The applied art, taken alone or in combination, does not teach or suggest a method for offloading hardware interrupt processing from a host system to a subsystem wherein, among other features, "...said subsystem hardware includes a status indicator containing status information relating to a plurality of operations being carried out on said subsystem hardware", as recited in independent claim 29.

The Examiner offers context registers 42 in FIG. 2 as teaching a status indicator containing status information relating to a plurality of operations being carried out on the subsystem hardware. In reality, context registers 42 store all of the cogenerator attributes, and are shown in FIG. 6. These attributes define the current state of the cogenerator 10. The current state may include a large number of parameters such as: cogenerator operational mode; draw pointer position; foreground color, background color; clipping window dimensions; etc. The contents of the context registers 42 are important as they define the personality of the cogenerator 10 at any given time and all attributes are user programmable. This gives a user considerable flexibility in operating the display system. *See* col. 6, lines 43-53.

Further, Peaslee's context registers 42 represent symbol attributes defining many functions that are needed to be performed in line with the current cogenerator state. *See* Peaslee at col. 14, lines 30-33.

Accordingly, Applicants submit that Peaslee's "attributes" are not equivalent to the recited "status indicator containing status information relating to a plurality of operations being carried out on said subsystem hardware."

3. **"Said subsystem...issues...instructions in response to...status information"**

The applied art, taken alone or in combination, does not teach or suggest a method for offloading hardware interrupt processing from a host system to a subsystem wherein, among other features, "...said subsystem processor monitors said status indicator and issues said captured instructions in response to said status information", as also recited in independent claim 29.

The deficiencies of the applied art with respect to the recited "status indicator containing status information relating to plurality of operations being carried out on said subsystem hardware" have been discussed above.

Contrary to the Examiner's assertions, Peaslee (col. 7, lines 13-27) does not teach or suggest ***issuing any captured instructions*** in response to the status information.

What Peaslee does teach in the cited section is that, once the attribute bus is selected for input to the display memory interface unit 35, the command interpreter in the display list processor 28 sends the attribute select code to the context registers 42. The interpreter cycles through 21 codes to extract all 21 attribute register values out of the context registers 42. This happens sequentially to perform a PUSH operation. The attribute select code connects to the attribute multiplexer 93 in the context registers 42. The first code sent selects attribute register 1 for output. The attribute multiplexer 93 drives the data to the readback multiplexer 44. The first attribute value is at the input to the display memory interface unit 35. The command interpreter in the display list processor 28 controls the attribute stack address generator 96. Thus, Peaslee's context registers contain data that is pushed to display memory interface unit 35 through attribute multiplexer 103 and readback multiplexer 44. *See* Peaslee col. 7, lines 13-27 and FIGS. 2 and 6. Data is pushed, and "captured instructions" are not issued.

B. Claim 34

1. "Status registers each...indicate a status of a different...graphics operation"

The applied art, taken alone or in combination, does not teach or suggest a computer system suitable for graphics rendering wherein, among other features, "...said graphics accelerator includes a plurality of status registers which each indicate a status of a different one of a plurality of graphics operations", as recited in independent claim 34.

In the interests of brevity, Applicants invite the Examiner's attention to paragraph 1. A. 2. above, from which the deficiencies of the applied art in this regard have been identified.

2. "interrupt generation and handling...by the...subsystem and not by the CPU"

The applied art, taken alone or in combination, does not teach or suggest a computer system suitable for graphics rendering wherein, among other features, "...hardware interrupt generation and handling is accomplished by the graphics subsystem and not by the CPU", as also recited in independent claim 34.

In the interests of brevity, Applicants invite the Examiner's attention to paragraph I. A. 1. above, from which the deficiencies of the applied art in this regard have been identified.

Whether or not Peaslee discloses handling interrupts via the DLP 28, Peaslee at least teaches that it is necessary for the CPU to generate interrupts, in contradiction to Applicants' recited invention, wherein interrupt ***generation and handling*** is accomplished by the graphics subsystem and not the CPU.

II. Motivation is Lacking -- Peaslee Teaches Away

Applicants submit that a person with skill in the art would not be motivated to combine Peaslee and Dye in the manner suggested to form Applicants' claimed invention, since Peaslee teaches away, at least by teaching that the CPU generates the hardware interrupt, as discussed above, even if DLP 28 handles the interrupt.

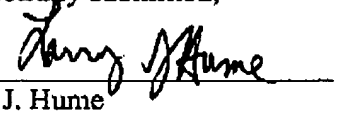
Applicants submit that having the CPU ***generate*** the interrupt is in direct contradiction to not only an objective of the present application, but the explicit language of the independent claims.

Application No.: 10/665,289 Docket No.: 21806-00056-US1

Conclusion

The Examiner has not met his burden in establishing a *prima facie* case of unpatentability not only because the combination of applied art does not teach or suggest all the claimed limitations, as discussed above, but because of deficient motivation to combine the references in the manner suggested by the Examiner. Withdrawal of the rejections and allowance of claims 29-37 are respectfully requested.

Respectfully submitted,

By 

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